



PATENT
Attorney Docket No. ASC-023DVC2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS: Fitzgerald
SERIAL NO.: 10/022,689 GROUP NO.: 2813
FILING DATE: December 17, 2001 EXAMINER: Laura M. Schillinger
TITLE: CONTROLLING THREADING DISLOCATION DENSITIES IN GE
ON SI USING GRADED GESI LAYERS AND PLANARIZATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with the provisions of 37 C.F.R. 1.97 and 1.98, Applicants hereby make of record the patents and publications listed on the accompanying Form PTO-1449, and other information contained herein, for consideration by the Examiner in connection with the examination of the above-identified patent application. Copies of the patents and publications are enclosed.

REMARKS

In accordance with the provisions of 37 C.F.R. 1.97, this statement is being filed (CHECK ONE):

- ☐ (1) within three (3) months of the **filing date** of a national application other than a continued prosecution application under 37 C.F.R. 1.53(d), or within three (3) months of the **date of entry of the national stage** as set forth in 37 C.F.R. 1.491 in an international application, or before the mailing of the **first Office action** on the merits, or before the mailing of a **first Office action** after the filing of a request for continued examination under 37 C.F.R. 1.114; or
- ☒ (2) after the period defined in (1) but before the mailing date of a **final action** or a **notice of allowance** under 37 C.F.R. 1.311, and
- ☐ the requisite Statement is below, **OR**
- ☒ the requisite fee under 37 C.F.R. 1.17(p), namely **\$180.00**, is included herein, or

- ☐ (3) after the mailing date of a **final action** or **notice of allowance** but before the payment of the **issue fee**, **AND**
- ☐ the requisite Statement is below, **AND**
- ☐ the requisite petition fee under 37 C.F.R. 1.17(p), namely **\$180.00** is included herein.

In addition, Applicant wishes to inform the Examiner about the following co-pending patent applications, publications, issued patents, and Office Actions issued therein:

U.S. Serial No. 10/264,935, filed on October 4, 2002, by Lochtefeld et al.;

U.S. Serial No. 10/456,708, filed on 06/06/2003, by Lochtefeld et al.;

U.S. Serial No. 10/456,103, filed on 06/06/2003, by Lochtefeld et al.;

U.S. Publication No. 2003-0102498-A1, published 06/05/2003, by Braithwaite et al.;

U.S. Serial No. 10/389,003, filed 03/14/2003, by Fitzgerald;

U.S. Patent No. 6,107,653, issued 08/22/2000, by Fitzgerald;

U.S. Patent No. 6,291,321, issued 09/18/2001, by Fitzgerald;

U.S. Serial No. 09/611,024, filed 07/06/2000, by Fitzgerald;

U.S. Patent No. 6,573,126, issued 06/03/2003, by Cheng et al.;

U.S. Serial No. 10/384,160, filed 03/07/2003, by Cheng et al.;

U.S. Serial No. 10/379,355, filed 03/04/2003, by Cheng et al.;

U.S. Patent No. 6,602,613, issued 08/05/2003, by Fitzgerald;

U.S. Serial No. 10/391,086, filed on 03/18/2003, by Fitzgerald;

U.S. Serial No. 09/764,177, filed on 01/07/2001, by Fitzgerald;

U.S. Publication No. 2002-0100942 A1, published 08/01/2002, by Fitzgerald et al.;

U.S. Publication No. 2002-0125471, published 09/12/2002, by Fitzgerald et al.;

U.S. Publication No. 2003-0034529, published 02/20/2003, by Fitzgerald et al.;

U.S. Serial No. 10/625,018, filed 07/23/2003, by Fitzgerald et al.;

U.S. Publication No. 2002-0123197, published 07/05/2002, by Fitzgerald et al.;

U.S. Serial No. 10/611,739, filed 07/01/2003, by Fitzgerald et al.;

U.S. Publication No. 2002-0125497, published 09/12/2002, by Fitzgerald;

U.S. Serial No. 09/906,545, filed on 07/16/2001, by Fitzgerald;

U.S. Serial No. 09/906,200, filed 07/16/2001, by Fitzgerald; and

U.S. Publication No. 2003-0077867, published 07/24/2003, by Fitzgerald.


It is respectfully requested that each of the patents and publications listed on the attached Form PTO-1449, and other information contained herein, be made of record in this application.

Respectfully submitted,

Date: August 13, 2003
Reg. No. 44,381

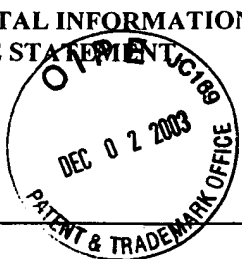
Tel. No.: (617) 310-8327
Fax No.: (617) 248-7100

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Natasha C. Us
Attorney for the Applicant
Testa, Hurwitz, & Thibault, LLP
High Street Tower
125 High Street
Boston, Massachusetts 02110

FORM PTO - 1449

SUPPLEMENTAL INFORMATION
DISCLOSURE STATEMENT

ATTY DOCKET NO.: ASC-023DVC2

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U.S. PATENT DOCUMENTS

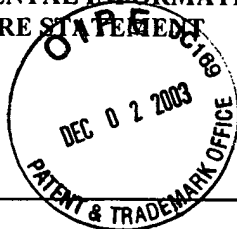
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	A1	4,010,045	03/01/1977	Ruehrwein			
	A2	4,710,788	12/01/1987	Dambkes et al.			
	A3	4,987,462	01/22/1991	Kim et al.			
	A4	4,990,979	02/05/1991	Otto			
	A5	5,013,681	05/07/1991	Godbey et al.			
	A6	5,155,571	10/13/1992	Wang et al.			
	A7	5,166,084	11/24/1992	Pfiester			
	A8	5,202,284	04/01/1993	Kamins et al.			
	A9	5,207,864	05/04/1993	Bhat et al.			
	A10	5,208,182	05/04/1993	Narayan et al.			
	A11	5,212,110	05/18/1993	Pfiester et al.			
	A12	5,221,413	06/22/1993	Brasen et al.			
	A13	5,241,197	08/31/1993	Murakami et al.			
	A14	5,285,086	02/08/1994	Fitzgerald, Jr.			
	A15	5,291,439	03/01/1994	Kauffmann, et al.			
	A16	5,310,451	05/10/1994	Tejwani et al.			
	A17	5,316,958	05/31/1994	Meyerson			
	A18	5,346,848	09/13/1994	Gruppen-Shemansky et al.			
	A19	5,374,564	12/20/1994	Bruel			
	A20	5,413,679	05/09/1995	Godbey			
	A21	5,426,069	06/20/1995	Selvakumar et al.			
	A22	5,426,316	06/20/1995	Mohammad			
	A23	5,461,243	10/24/1995	Ek et al.			
	A24	5,461,250	10/24/1995	Burghartz et al.			
	A25	5,462,883	10/31/1995	Dennard et al.			
	A26	5,476,813	12/19/1995	Naruse			
	A27	5,479,033	12/26/1995	Baca et al.			
	A28	5,484,664	01/16/1996	Kitahara et al.			
	A29	5,523,243	06/04/1996	Mohammad			
	A30	5,523,592	06/04/1996	Nakagawa et al.			

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U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A31	5,536,361	07/16/1996	Kondo et al.			
	A32	5,540,785	07/30/1996	Dennard et al.			
	A33	5,596,527	01/12/1997	Tomioka, et al.			
	A34	5,617,351	04/01/1997	Bertin, et al.			
	A35	5,683,934	11/04/1997	Candelaria			
	A36	5,698,869	12/16/1997	Yoshimi et al.			
	A37	5,728,623	03/17/1998	Mori			
	A38	5,739,567	04/14/1998	Wong			
	A39	5,759,898	06/02/1998	Ek et al.			
	A40	5,777,347	07/07/1998	Bartelink			
	A41	5,786,612	07/28/1998	Otani et al.			
	A42	5,786,614	07/28/1998	Chuang, et al.			
	A43	5,792,679	08/11/1998	Nakato			
	A44	5,808,344	09/15/1998	Ismail et al.			
	A45	5,847,419	12/08/1998	Imai et al.			
	A46	5,877,070	03/02/1999	Goesele et al.			
	A47	5,906,708	05/25/1999	Robinson et al.			
	A48	5,912,479	06/15/1999	Mori et al.			
	A49	5,943,560	08/24/1999	Chang et al.			
	A50	5,963,817	10/05/1999	Chu et al.			
	A51	5,966,622	10/12/1999	Levine et al.			
	A52	5,998,807	12/07/1999	Lustig et al.			
	A53	6,013,134	01/11/2000	Chu et al.			
	A54	6,033,974	03/07/2000	Henley et al.			
	A55	6,033,995	03/07/2000	Muller			
	A56	6,058,044	05/02/2000	Sugiura et al.			
	A57	6,074,919	06/13/2000	Gardner et al.			
	A58	6,096,590	08/01/2000	Chan et al.			
	A59	6,103,559	08/15/2000	Gardner et al.			
	A60	6,111,267	08/29/2000	Fischer et al.			

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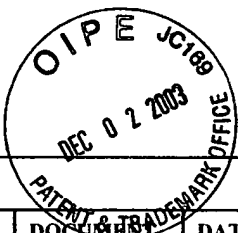
U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A61	6,117,750	09/12/2000	Bensahel et al.			
	A62	6,130,453	10/10/2000	Mei, et al.			
	A63	6,133,799	10/17/2000	Favors, Jr., et al.			
	A64	6,140,687	10/31/2000	Shimomura et al.			
	A65	6,143,636	11/07/2000	Forbes, et al.			
	A66	6,153,495	11/28/2000	Kub et al.			
	A67	6,154,475	11/28/2000	Soref et al.			
	A68	6,160,303	12/12/2000	Fattaruso			
	A69	6,162,688	12/19/2000	Gardner et al.			
	A70	6,184,111	02/06/2001	Henley et al.			
	A71	6,191,007	02/20/2001	Matsui et al.			
	A72	6,191,432	02/20/2001	Sugiyama et al.			
	A73	6,194,722	02/27/2001	Fiorini et al.			
	A74	6,204,529	03/20/2001	Lung, et al.			
	A75	6,207,977	03/01/2001	Augusto			
	A76	6,210,988	04/03/2001	Howe et al.			
	A77	6,218,677	04/17/2001	Broekaert			
	A78	6,232,138	05/15/2001	Fitzgerald et al.			
	A79	6,235,567	05/22/2001	Huang			
	A80	6,242,324	06/05/2001	Kub et al.			
	A81	6,249,022	06/19/2001	Lin, et al.			
	A82	6,251,755	06/26/2001	Furukawa et al.			
	A83	6,261,929	07/01/2001	Gehrke et al.			
	A84	6,266,278	07/24/2001	Harari, et al.			
	A85	6,271,551	08/07/2001	Schmitz et al.			
	A86	6,271,726	08/07/2001	Fransis et al.			
	A87	6,313,016	11/06/2001	Kibbel et al.			
	A88	6,316,301	11/13/2001	Kant			
	A89	6,323,108	11/27/2001	Kub et al.			
	A90	6,329,063	12/11/2001	Lo et al.			

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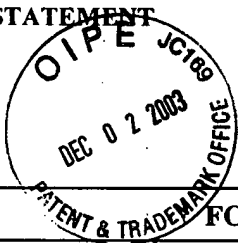
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 U.S. PATENT DOCUMENTS							
EXAM. INIT.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE	
	A91	6,335,546	01/01/2002	Tsuda et al.		07/30/1999	
	A92	6,339,232	01/15/2002	Takagi		09/20/1999	
	A93	6,368,733	04/09/2002	Nishinaga		08/05/1999	
	A94	6,372,356	04/16/2002	Thornton et al.		04/028/2000	
	A95	6,399,970	06/04/2002	Kubo et al.		09/16/1997	
	A96	6,407,406	06/18/2002	Tezuka		06/29/1999	
	A97	6,425,951	07/30/2002	Chu et al.		08/06/1999	
	A98	6,429,061	08/06/2002	Rim		07/26/2000	
	A99	6,420,937	07/16/2002	Akatsuka et al.		06/14/2001	
	A100	6,521,041	02/18/2003	Wu et al.		04/09/1999	
	A101	6,555,839	04/29/2003	Fitzgerald		05/16/2001	
	A102	6,583,015	06/24/2003	Fitzgerald et al.		08/06/2001	
	A103	6,521,041	02/18/2003	Wu et al.		04/09/1999	
	A104	2001/0003364	06/14/2001	Sugawara et al.		12/08/2000	
	A105	2002/0043660	04/18/2002	Yamazaki et al.		06/25/2001	
	A106	6,593,191	07/15/2003	Fitzgerald		05/16/2001	
	A107	6,573,126	06/03/2003	Cheng et al.		08/10/2001	
	A108	2002/0096717	07/25/2002	Chu et al.		01/25/2001	
	A109	2002/0100942	08/01/2001	Fitzgerald et al.		06/19/2001	
	A110	2002/0123167	09/05/2002	Fitzgerald		07/16/2001	
	A111	2002/0123183	09/05/2002	Fitzgerald		07/16/2001	
	A112	2002/0123197	09/05/2002	Fitzgerald et al.		06/19/2001	
	A113	2002/0125471	09/12/2002	Fitzgerald et al.		12/04/2001	
	A114	2002/0125497	09/12/2002	Fitzgerald		07/16/2001	
	A115	6,603,156	08/05/2003	Rim		03/31/2001	
	A116	2003/0003679	01/02/2003	Doyle et al.		06/29/2001	

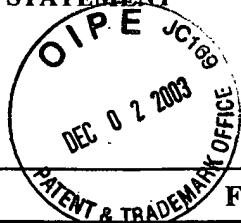
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 FOREIGN PATENT DOCUMENTS									
EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B1	41 01 167	07/23/1992	DE				NO	NO
	B2	0 587 520	03/16/1994	EP				NO	YES
	B3	0 683 522	11/22/1995	EP				NO	YES
	B4	0 828 296	03/11/1998	EP				NO	YES
	B5	0 829 908	03/18/1998	EP				NO	YES
	B6	0 838 858	04/29/1998	EP				NO	NO
	B7	1 020 900	07/19/2000	EP				NO	YES
	B8	1 174 928	01/23/2002	EP				NO	YES
	B9	2 342 777	04/19/2000	GB				YES	YES
	B10	10-270685	10/09/1998	JP				NO	YES
	B11	11-233744	08/27/1999	JP				NO	NO
	B12	2000-021783	08/31/2000	JP				NO	YES
	B13	2000-031491	01/28/2000	JP				NO	NO
	B14	2001-319935	11/16/2001	JP				NO	YES
	B15	2002-076334	03/15/2002	JP				NO	YES
	B16	2002-164520	06/07/2002	JP				NO	YES
	B17	2002-289533	10/04/2002	JP				NO	YES
	B18	4-307974	10/30/1992	JP				NO	NO
	B19	5-166724	07/02/1993	JP				NO	Abstract Only
	B20	6-177046	06/24/1994	JP				NO	Abstract Only
	B21	7-106446	04/21/1995	JP				NO	NO
	B22	7-240372	09/12/1995	JP				NO	Abstract Only
	B23	00/48239	08/17/2000	WO				NO	YES
	B24	00/54338	09/14/2000	WO				NO	YES

EXAMINER	DATE CONSIDERED
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FORM PTO - 1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY DOCKET NO.: ASC-023DVC2 APPLICANTS: Fitzgerald SERIAL NO.: 10/022,689 FILING DATE: December 17, 2001 GROUP: 2813
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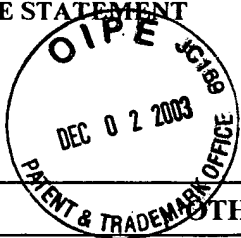


FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B25	01/022482	03/29/2001	WO				NO	YES
	B26	01/54202	07/26/2001	WO				NO	YES
	B27	01/93338	12/06/2001	WO				NO	YES
	B28	01/99169	12/27/2001	WO				NO	YES
	B29	02/071488	09/12/2002	WO				NO	YES
	B30	02/071491	09/12/2002	WO				NO	YES
	B31	02/071495	09/12/2002	WO				NO	YES
	B32	02/082514	10/17/2002	WO				NO	YES
	B33	02/13262	02/14/2002	WO				NO	YES
	B34	02/15244	02/21/2002	WO				NO	YES
	B35	02/27783	04/04/2002	WO				NO	YES
	B36	02/47168	06/13/2002	WO				NO	YES
	B37	98/59365	12/30/1998	WO				NO	YES
	B38	99/53539	10/21/1999	WO				NO	YES
	B39	6-252046	11/19/1992	JP				NO	YES


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OTHER ART, JOURNAL ARTICLES, ETC.		
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C1	Armstrong et al., "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," IEDM Technical Digest (1995 International Electron Devices Meeting) pp. 761-764.
	C2	Armstrong, "Technology for SiGe Heterostructure-Based CMOS Devices", PhD Thesis, Massachusetts Institute of Technology, 1999, pp. 1-154.
	C3	Augusto et al., "Proposal for a New Process Flow for the Fabrication of Silicon-based Complementary MOD-MOSFETs without ion Implantation," Thin Solid Films, vol. 294, no. 1-2, pp. 254-258 (February 15, 1997).
	C4	Barradas et al., "RBS analysis of MBE-grown SiGe/(001) Si heterostructures with thin, high Ge content SiGe channels for HMOS transistors," Modern Physics Letters B (2001) (abstract).
	C5	Borenstein et al., "A New Ultra-Hard Etch-Stop Layer for High Precision Micromachining," Proceedings of the 1999 12th IEEE International Conference on Micro Electro Mechanical Systems (MEMS) (January 17-21, 1999) pp. 205-210.
	C6	Bouillon et al., "Search for the optimal channel architecture for 0.18/0.12 μ m bulk CMOS Experimental study," IEEE, (1996) pp. 21.2.1-21.2.4.
	C7	Bruel et al., "@SMART CUT: A Promising New SOI Material Technology," Proceedings 1995 IEEE International SOI Conference (October 1995) pp. 178-179.
	C8	Bruel, "Silicon on Insulator Material Technology," Electronic Letters, Vol. 13, No. 14 (July 6, 1995) pp. 1201-1202.
	C9	Bufler et al., "Hole transport in strained Si _{1-x} Ge _x alloys on Si _{1-y} Ge _y substrates," Journal of Applied Physics, Vol. 84, No. 10 (November 15, 1998) pp. 5597-5602.
	C10	Burghartz et al., "Microwave Inductors and Capacitors in Standard Multilevel Interconnect Silicon Technology", IEEE Transactions on Microwave Theory and Techniques, Vol. 44, No. 1, January 1996, pp. 100-104.
	C11	Canaperi et al., "Preparation of a relaxed Si-Ge layer on an insulator in fabricating high-speed semiconductor devices with strained epitaxial films," International Business Machines Corporation, USA (2002) (abstract).
	C12	Carlin et al., "High Efficiency GaAs-on-Si Solar Cells with High Voc Using Graded GeSi Buffers," IEEE (2000) pp. 1006-1011
	C13	Chang et al., "Selective Etching of SiGe/Si Heterostructures," Journal of the Electrochemical Society, No. 1 (January 1991) pp. 202-204.
	C14	Cheng et al., "Electron Mobility Enhancement in Strained-Si n-MOSFETs Fabricated on SiGe-on-Insulator (SGOI) Substrates," IEEE Electron Device Letters, Vol. 22, No. 7 (July 2001) pp. 321-323.
	C15	Cheng et al., "Relaxed Silicon-Germanium on Insulator Substrate by Layer Transfer," Journal of Electronic Materials, Vol. 30, No. 12 (2001) pp. L37-L39.

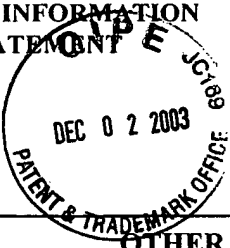
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OTHER ART, JOURNAL ARTICLES, ETC.			
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)		
	C16	Cullis et al, "Growth ripples upon strained SiGe epitaxial layers on Si and misfit dislocation interactions," Journal of Vacuum Science and Technology A, Vol. 12, No. 4 (July/August 1994) pp. 1924-1931.	
	C17	Currie et al., "Carrier mobilities and process stability of strained S in- and p-MOSFETs on SiGe virtual substrates," J. Vac. Sci. Technol. B., Vol. 19, No. 6 (Nov/Dec 2001) pp. 2268-2279.	
	C18	Eaglesham et al., "Dislocation-Free Stranski-Krastanow Growth of Ge on Si(100)," Physical Review Letters, Vol. 64, No. 16 (April 16, 1990) pp. 1943-1946.	
	C19	Feijoo et al., "Epitaxial Si-Ge Etch Stop Layers with Ethylene Diamine Pyrocatechol for Bonded and Etchback Silicon-on-Insulator," Journal of Electronic Materials, Vol. 23, No. 6 (June 1994) pp. 493-496.	
	C20	Fischetti et al., "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," J. Appl. Phys., Vol. 80, No. 4 (August 15, 1996) pp. 2234-2252.	
	C21	Fischetti, "Long-range Coulomb interactions in small Si devices. Part II. Effective electronmobility in thin-oxide structures," Journal of Applied Physics, Vol. 89, No. 2 (January 15, 2001) pp. 1232-1250.	
	C22	Fitzgerald et al., "Dislocation dynamics in relaxed graded composition semiconductors," Materials Science and Engineering B67, (1999) pp. 53-61.	
	C23	Fitzgerald et al., "Relaxed GexSi1-x structures for III-V integration with Si and high mobility two-dimensional electron gases in Si," AT&T Bell Laboratories, Murray Hill, NJ 07974 (1992) American Vacuum Society, pp. 1807-1819	
	C24	Fitzgerald et al., "Totally Relaxed GexSi1-x Layers with Low Threading Dislocation Densities Grown on Si Substrates," Applied Physics Letters, Vol. 59, No. 7 (August 12, 1991) pp. 811-813.	
	C25	Garone et al., "Silicon vapor phase epitaxial growth catalysis by the presence of germane," Applied Physics Letters, Vol. 56, No. 13 (March 26, 1990) pp. 1275-1277.	
	C26	Gray and Meyer, "Analysis and Design of Analog Integrated Circuits", John Wiley & Sons, 1984, pp. 605-632.	
	C27	Grützmacher et al., "Ge segregation in SiGe/Si heterostructures and its dependence on deposition technique and growth atmosphere," Applied Physics Letters, Vol. 63, No. 18 (November 1, 1993) pp. 2531-2533.	
	C28	Hackbarth et al., "Alternatives to thick MBE-grown relaxed SiGe buffers," Thin Solid Films, Vol. 369, No. 1-2 (July 2000) pp. 148-151.	
	C29	Hackbarth et al., "Strain relieved SiGe buffers for Si-based heterostructure field-effect transistors," Journal of Crystal Growth, Vol. 201/202 (1999) pp. 734-738.	
	C30	Herzog et al., "SiGe-based FETs: buffer issues and device results," Thin Solid Films, Vol. 380 (2000) pp. 36-41.	
	C31	Höck et al., "Carrier mobilities in modulation doped Si1-xGex heterostructures with respect to FET applications," Thin Solid Films, Vol. 336 (1998) pp. 141-144.	

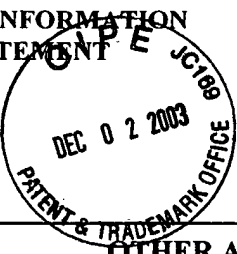
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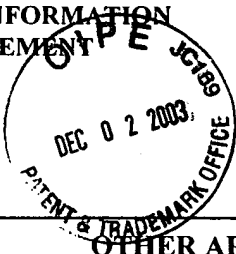
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OTHER ART, JOURNAL ARTICLES, ETC.		
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C32	Höck et al., "High hole mobility in Si _{0.17} Ge _{0.83} channel metal-oxide-semiconductor field-effect transistors grown by plasma-enhanced chemical vapor deposition," Applied Physics Letters, Volume 76, No. 26 (June 26, 2000) pp. 3920-3922.
	C33	Höck et al., "High performance 0.25 µm p-type Ge/SiGe MODFETs," Electronics Letters, Vol. 34, No. 19 (September 17, 1998) pp. 1888-1889.
	C34	Huang et al., "High-quality strain-relaxed SiGe alloy grown on implanted silicon-on-insulator substrate," Applied Physics Letters, Vol. 76, No. 19 (May 8, 2000) pp. 2680-2682.
	C35	Huang et al., "The Impact of Scaling Down to Deep Submicron on CMOS RF Circuits", IEEE Journal of Solid-State Circuits, Vol. 33, No. 7, July, 1998, pp. 1023-1036.
	C36	IBM Technical Disclosure Bulletin, Vol. 35, No. 4B (September 1992), "2 Bit/Cell EEPROM Cell Using Band to Band Tunneling for Data Read-Out," pp. 136-140.
	C37	IBM Technical Disclosure Bulletin, Volume 32, No. 8A, January 1990, "Optimal Growth Technique and Structure for Strain Relaxation of Si-Ge Layers on Si Substrates", pp. 330-331.
	C38	Ishikawa et al., "Creation of Si-Ge-based SIMOX structures by low energy oxygen implantation," Proceedings 1997 IEEE International SOI Conference (October 1997) pp. 16-17.
	C39	Ishikawa et al., "SiGe-on-insulator substrate using SiGe alloy grown Si(001)," Applied Physics Letters, Vol. 75, No. 7 (August 16, 1999) pp. 983-985.
	C40	Ismail et al., "Modulation-doped n-type Si/SiGe with inverted interface," Appl. Phys. Lett., Vol. 65, No. 10 (September 5, 1994) pp. 1248-1250.
	C41	Ismail, "Si/SiGe High-Speed Field-Effect Transistors," Electron Devices Meeting, Washington, D.C. (December 10, 1995) pp. 20.1.1-20.1.4.
	C42	Kearney et al., "The effect of alloy scattering on the mobility of holes in a Si _{1-x} Ge _x quantum well," Semicond. Sci Technol., Vol. 13 (1998) pp. 174-180.
	C43	Kim et al., "A Fully Integrated 1.9-GHz CMOS Low-Noise Amplifier", IEEE Microwave and Guided Wave Letters, Vol. 8, No. 8, August 1998, pp. 293-295.
	C44	Koester et al., "Extremely High Transconductance Ge/Si _{0.4} Ge _{0.6} p-MODFET's Grown by UHV-CVD," IEEE Electron Device Letters, Vol. 21, No. 3 (March 2000) pp. 110-112.
	C45	König et al., "Design Rules for n-Type SiGe Hetero FETs," Solid State Electronics, Vol. 41, No. 10 (1997), pp. 1541-1547.
	C46	König et al., "p-Type Ge-Channel MODFET's with High Transconductance Grown on Si Substrates," IEEE Electron Device Letters, Vol. 14, No. 4 (April 1993) pp. 205-207.
	C47	König et al., "SiGe HBTs and HFETs," Solid-State Electronics, Vol. 38, No. 9 (1995) pp. 1595-1602.
	C48	Kuznetsov et al., "Technology for high-performance n-channel SiGe modulation-doped field-effect transistors," J. Vac. Sci. Technol., B 13(6), pp. 2892-2896 (November/December 1995).
	C49	Larson, "Integrated Circuit Technology Options for RFIC's □ Present Status and Future Directions", IEEE Journal of Solid-State Circuits, Vol. 33, No. 3, March 1998, pp. 387-399.

EXAMINER

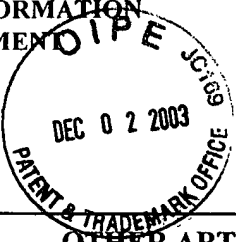
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	C50	Lee and Wong, "CMOS RF Integrated Circuits at 5 GHz and Beyond", Proceedings of the IEEE, Vol. 88, No. 10, October 2000, pp. 1560-1571.
	C51	Lee et al., "Strained Ge channel p-type metal-oxide-semiconductor field-effect transistors grown on Si _{1-x} Gex/Si virtual substrates," Applied Physics Letters, Vol. 79, No. 20 (November 12, 2001) pp. 3344-3346.
	C52	Lee et al., "Strained Ge channel p-type MOSFETs fabricated on Si _{1-x} Gex/Si virtual substrates," Mat. Res. Soc. Symp. Proc., Vol. 686 (2002) pp. A1.9.1-A1.9.5.
	C53	Leitz et al., "Channel Engineering of SiGe-Based Heterostructures for High Mobility MOSFETs," Mat. Res. Soc. Symp. Proc., Vol. 686 (2002) pp. A3.10.1-A3.10.6.
	C54	Leitz et al., "Dislocation glide and blocking kinetics in compositionally graded SiGe/Si," Journal of Applied Physics, Vol. 90, No. 6 (September 15, 2001) pp. 2730-2736.
	C55	Leitz et al., "Hole mobility enhancements in strained Si/Si _{1-y} Gey p-type metal-oxide-semiconductor field-effect transistors grown on relaxed Si _{1-x} Gex (x<y) virtual substrates," Applied Physics Letters, Vol. 79, No. 25 (December 17, 2001) pp. 4246-4248.
	C56	Li et al., "Design of high speed Si/SiGe heterojunction complementary metal-oxide-semiconductor field effect transistors with reduced short-channel effects," J. Vac. Sci. Technol., A Vol. 20 No.3 (May/June 2002) pp. 1030-1033.
	C57	Lu et al., "High Performance 0.1 μ m Gate-Length P-Type SiGe MODFET's and MOS-MODFET's," IEEE Transactions on Electron Devices, Vol. 47, No. 8, August 2000, pp. 1645-1652.
	C58	M. Kummer et al., "Low energy plasma enhanced chemical vapor deposition," Materials Science and Engineering B89 (2002) pp. 288-295.
	C59	Maiti et al., "Strained-Si heterostructure field effect transistors," Semicond. Sci. Technol., Vol. 13 (1998) pp. 1225-1246.
	C60	Maszara, "Silicon-On-Insulator by Wafer Bonding: A Review," Journal of the Electrochemical Society, No. 1 (January 1991) pp. 341-347.
	C61	Meyerson et al., "Cooperative Growth Phenomena in Silicon/Germanium Low-Temperature Epitaxy," Applied Physics Letters, Vol. 53, No. 25 (December 19, 1988) pp. 2555-2557.
	C62	Mizuno et al., "Advanced SOI-MOSFETs with Strained-Si Channel for High Speed CMOS-Electron/Hole Mobility Enhancement," 2002 Symposium on VLSI Technology, Digest of Technical Papers, Honolulu, (June 13-15), IEEE New York, NY, pp. 210-211.
	C63	Mizuno et al., "Electron and Hole Mobility Enhancement in Strained-Si MOSFET's on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," IEEE Electron Device Letters, Vol. 21, No. 5 (May 2000) pp. 230-232.
	C64	Mizuno et al., "High Performance Strained-Si p-MOSFETs on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," IEEE IDEM Technical Digest, (1999 International Electron Device Meeting) pp. 934-936.

EXAMINER	DATE CONSIDERED
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	C65	Nayak et al., "High-Mobility Strained-Si PMOSFET's"; IEEE Transactions on Electron Devices, Vol. 43, No. 10, October 1996, pp. 1709-1716.
	C66	O'Neill et al., "SiGe Virtual substrate N-channel heterojunction MOSFETS," Semicond. Sci. Technol., Vol. 14 (1999) pp. 784-789.
	C67	Papananos, "Radio-Frequency Microelectronic Circuits for Telecommunication Applications", Kluwer Academic Publishers, 1999, pp. 115-117, 188-193.
	C68	O'ta, Y. et al., "Application of heterojunction FET to power amplifier for cellular telephone," ELECTRONIC LETTERS, IEE STEVANAGE, GB, Vol. 30 No. 11, 26 May 1994, pp. 906-907.
	C69	Parker et al., "SiGe heterostructure CMOS circuits and applications," Solid State Electronics, Vol. 43 (1999) pp. 1497-1506.
	C70	Ransom et al., "Gate-Self-Aligned n-channel and p-channel Germanium MOSFET's," IEEE Transactions on Electron Devices, Vol. 38, No. 12 (December 1991) pp. 2695.
	C71	Reinking et al., "Fabrication of high-mobility Ge p-channel MOSFETs on Si substrates," Electronics Letters, Vol. 35, No. 6 (March 18, 1999) pp. 503-504.
	C72	Rim et al., "Enhanced Hole Mobilities in Surface-channel Strained-Si p-MOSFETs"; IEDM, 1995, pp. 517-520.
	C73	Rim et al., "Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's"; IEEE Transactions on Electron Devices, Vol. 47, No. 7, July 2000, pp. 1406-1415.
	C74	Rim, "Application of Silicon-Based Heterostructures to Enhanced Mobility Metal-Oxide-Semiconductor Field-Effect Transistors", PhD Thesis, Stanford University, 1999; pp. 1-184.
	C75	Robbins et al., "A model for heterogeneous growth of Si _{1-x} Ge _x films for hydrides," Journal of Applied Physics, Vol. 69, No. 6 (March 15, 1991) pp. 3729-3732.
	C76	Sadek et al., "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," IEEE Trans. Electron Devices (August 1996) pp. 1224-1232.
	C77	Schäffler, "High-Mobility Si and Ge Structures," Semiconductor Science and Technology, Vol. 12 (1997) pp. 1515-1549.
	C78	Sugimoto and Ueno, "A 2V, 500 MHz and 3V, 920 MHz Low-Power Current-Mode 0.6 μ m CMOS VCO Circuit", IEICE Trans. Electron., Vol.E82-C, No. 7, July 1999, pp. 1327-1329.
	C79	Ternent et al., "Metal Gate Strained Silicon MOSFETs for Microwave Integrated Circuits", IEEE October 2000, pp. 38-43.
	C80	Tweet et al., "Factors determining the composition of strained GeSi layers grown with disilane and germane," Applied Physics Letters, Vol. 65, No. 20 (November 14, 1994) pp. 2579-2581.
	C81	Usami et al., "Spectroscopic study of Si-based quantum wells with neighboring confinement structure," Semicon. Sci. Technol. (1997) (abstract).
	C82	Welser et al., "Electron Mobility Enhancement in Strained-Si N-Type Metal-Oxide-Semiconductor Field-Effect Transistors," IEEE Electron Device Letters, Vol. 15, No. 3 (March 1994) pp. 100-102.

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	C83	Welser, "The Application of Strained Silicon/Relaxed Silicon Germanium Heterostructures to Metal-Oxide-Semiconductor Field-Effect Transistors," PhD Thesis, Stanford University, 1994, pp. 1-205.
	C84	Welser et al., "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," IEEE IDAM Technical Digest (1992 International Electron Devices Meeting) pp. 1000-1002.
	C85	Welser et al., "Evidence of Real-Space Hot-Electron Transfer in High Mobility, Strained-Si Multilayer MOSFETs," IEEE IDAM Technical Digest (1993 International Electron Devices Meeting) pp. 545-548.
	C86	Wolf and Tauber, Silicon Processing for the VLSI Era, Vol. 1: Process Technology, Lattice Press, Sunset Beach, CA, pp. 384-386 (1986).
	C87	Xie et al., "Semiconductor Surface Roughness: Dependence on Sign and Magnitude of Bulk Strain," The Physical Review Letters, Vol. 73, No. 22 (November 28, 1994) pp. 3006-3009.
	C88	Xie et al., "Very high mobility two-dimensional hole gas in Si/GeSi _{1-x} /Ge structures grown by molecular beam epitaxy," Appl. Phys. Lett., Vol. 63, No. 16 (October 18, 1993) pp. 2263-2264.
	C89	Xie, "SiGe Field effect transistors," Materials Science and Engineering, Vol. 25 (1999) pp. 89-121.
	C90	Yeo et al., "Nanoscale Ultra-Thin-Body Silicon-on-Insulator P-MOSFET with a SiGe/Si Heterostructure Channel," IEEE Electron Device Letters, Vol. 21, No. 4 (April 2000) pp. 161-163.
	C91	Zhang et al., "Demonstration of a GaAs-Based Compliant Substrate Using Wafer Bonding and Substrate Removal Techniques," Electronic Materials and Processing Research Laboratory, Department of Electrical Engineering, University Park, PA 16802 (1998) pp. 25-28.
	C92	Tsang et al., "Measurements of alloy composition and strain in thin Ge _x Si _{1-x} layers," J. Appl. Phys., Vol. 75 No. 12 (June 15, 1994) pp. 8098-8108.
	C93	Sakaguchi et al., "ELTRAN® by Splitting Porous Si Layers," Proc. 195 th Int. SOI Symposium, Vol. 99-3, Electrochemical Society (1999) pp. 117-121.
	C94	Yamagata et al., "Bonding, Splitting and Thinning by Porous Si in ELTRAN®, SOI-Epi Wafer™," Mat. Res. Soc. Symp. Proc., Vol. 681E (2001) pp. 18.2.1-18.2.10.

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